

# 10/100 Ethernet

PHY\_GND is a small plane that the ETH diff pairs should stay over

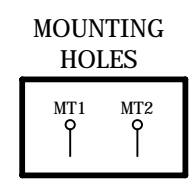
## Reset Latch

TI = DCK suffix  
 NXP = GW suffix  
 Fair = NC7SZ175P6  
 Fairchild is cheapest

## POR

### Strap Options

CLK\_OUT ICE mode (default high)  
 SPI\_MOSI Low = Little Indian  
 RAM\_CKE High = SPI Boot



# FPGA with 5000 LUTs

XP2-5 has:  
 5K LUTs 2 PLLs  
 9 blocks of 1Kx18 Block RAM  
 12 18x18 Multipliers  
 100 I/O with 144 pin package  
 "instant ON" = about 1.5 mS  
 input PLL clock = 10 MHz min

## Boot Straps

Mode 1	Mode 2	Boots from
1	1	NAND Flash
1	0	SD Card
0	1	Off-board Flash
0	0	Off-board Flash

MODE1 and MODE2 states and Board ID bits must be latched prior to UN\_RESET# pulsed

MODE1 and MODE2 have PU resistors

Use 1K ohm resistor to GND to set low

Pins 87 and 88 must be read prior to UN-RESET being pulsed

Pins 54 and 138 must be read prior to UN-RESET being pulsed

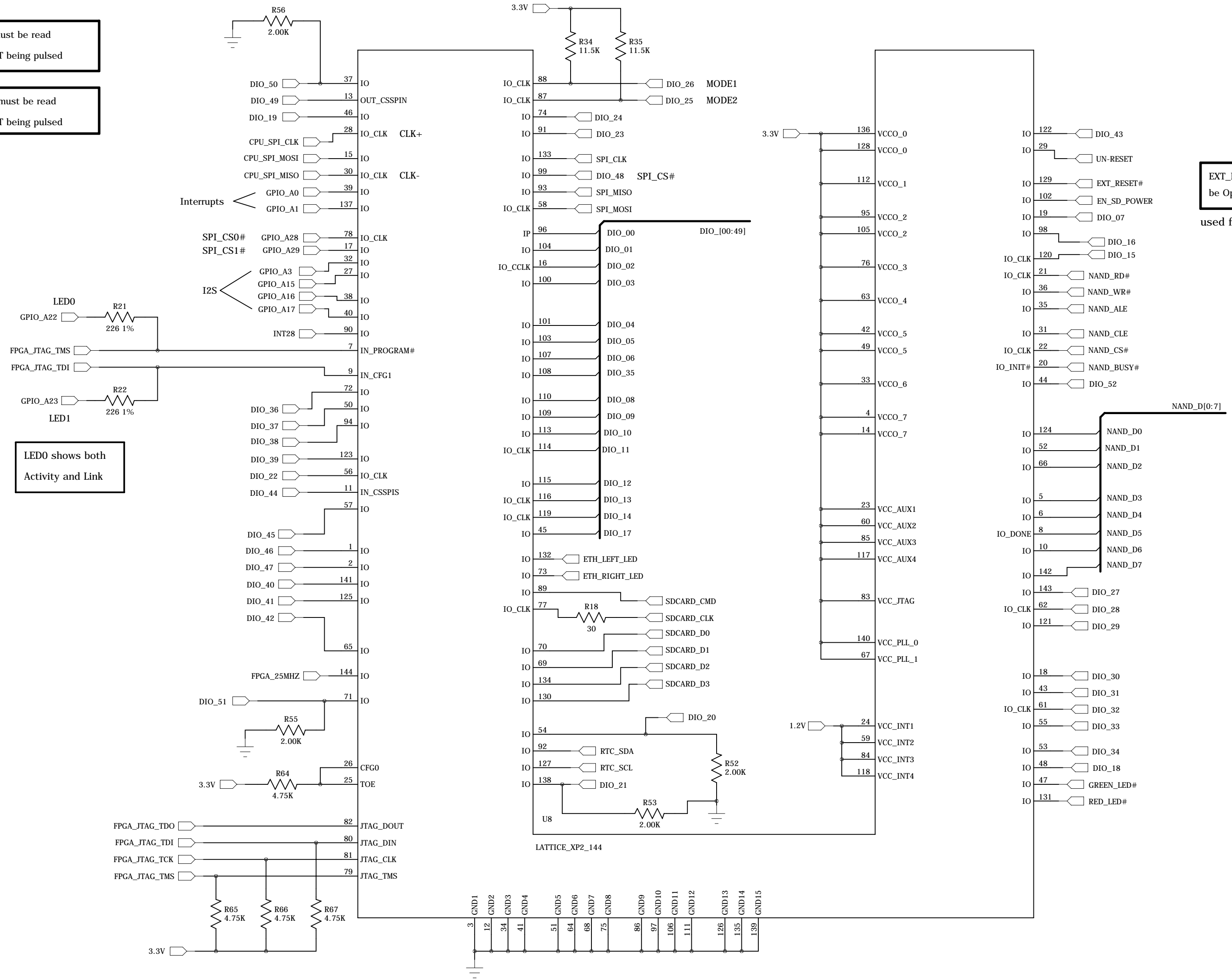
## Differences from TS-7500/7550/7551/7552

ETH LEDs are inverted  
 Console path not used

## Board ID bits

	Pin 54 (weak PU)	Pin 138 (weak PD)	Pin 71	Pin 37	Hex
TS-7500	1	1	1	1	F
TS-7550	1	1	0	1	B
WM-7551	0	0	1	1	C
TS-7552	1	0	1	1	D
TS-7553	1	0	0	1	9
TS-7554	0	0	0	1	8
TS-7555	0	1	0	1	A
TS-4500	0	0	0	0	0

7552 and 7553 FPGA pin 93 = MISO



EXT\_RESET# must be Open Drain used for WD reset

LED0 shows both Activity and Link

UN-RESET rising edge, deasserts CPU Reset (Must be careful at start up) It has a PD resistor -- always idle low  
 EN\_SD\_POWER should initialize high

During JTAG Flash programming the PROGRAM# pin should be high else it can inhibit Flash --> SRAM  
 DONE likewise must be high These do have weak PU resistors

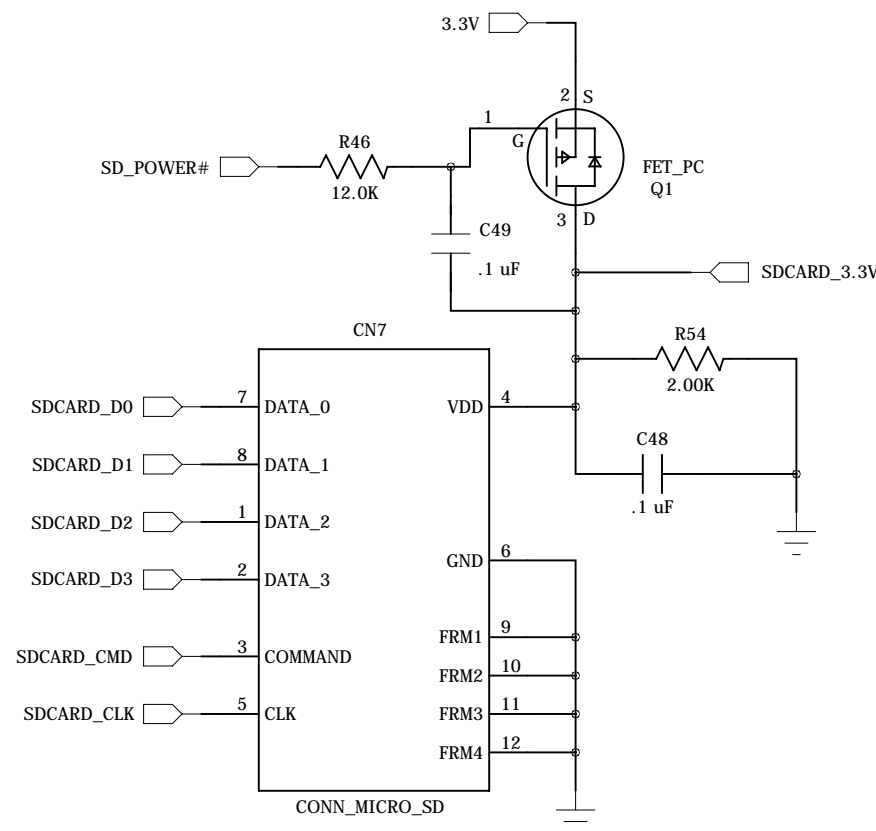
Set CONFIG\_MODE to NONE This allows all pins to be used

Pull-up and pull-down resistors are 6 to 30K ohms

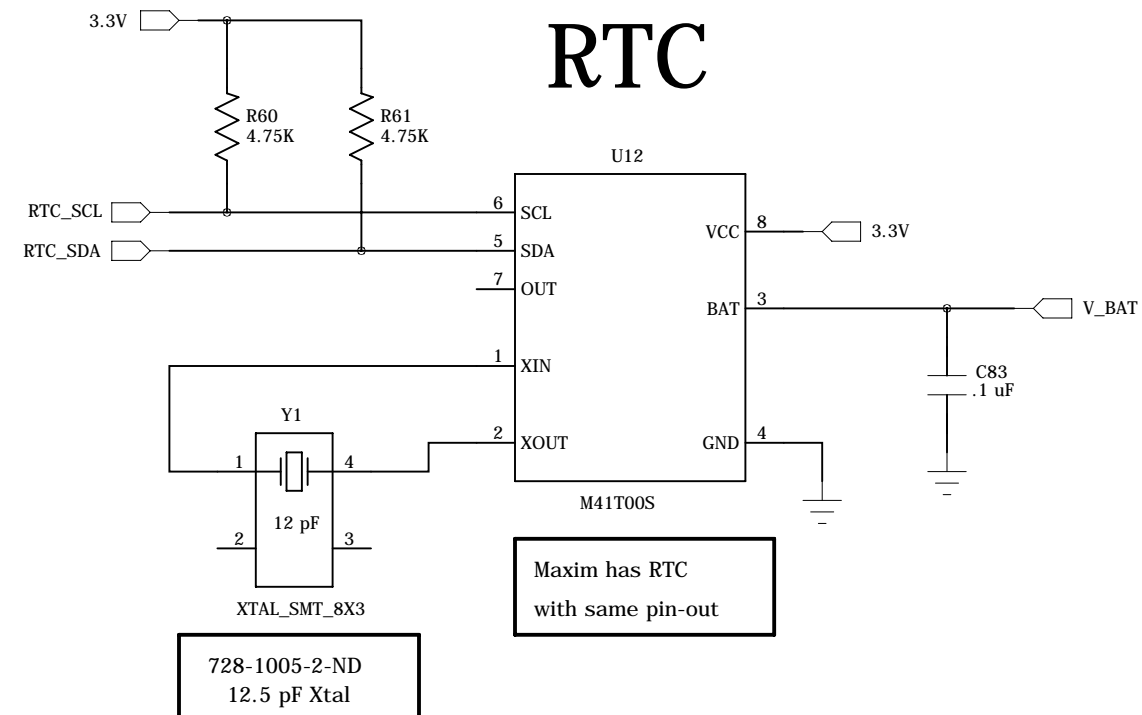
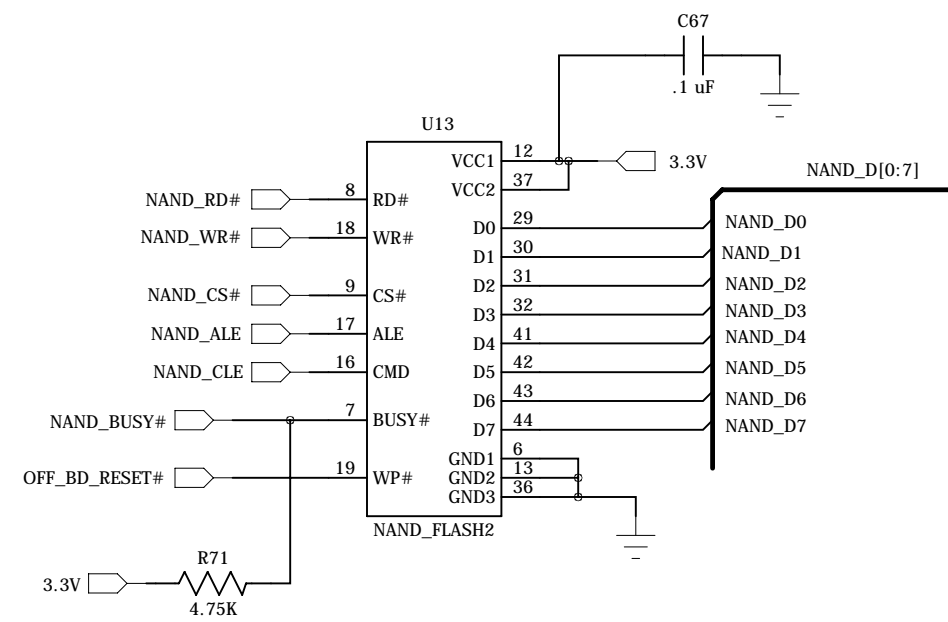
PROGRAM#, DONE, and INIT# are dedicated configuration pins when CFG0 is low. When CFG0 is high they are "general purpose I/O"  
 Page 4 of TN1141

Page 37 of Data Sheet (Hot Socketing)  
 Power Supplies can be sequenced in any order but must be monotonic  
 All I/O lines are tri-stated during power cycling

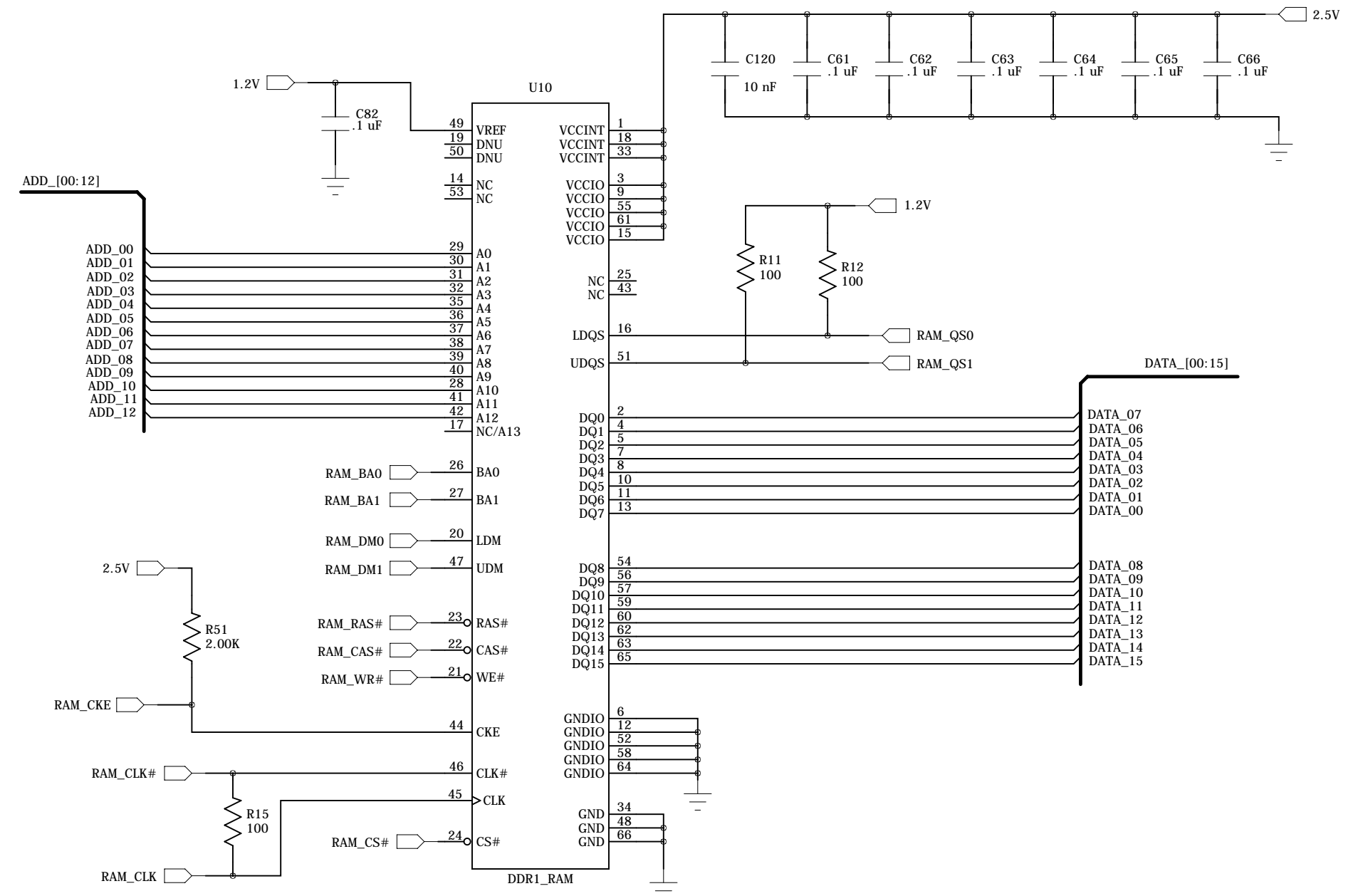
# Micro SD Card Socket



# 512 Mbyte NAND Flash



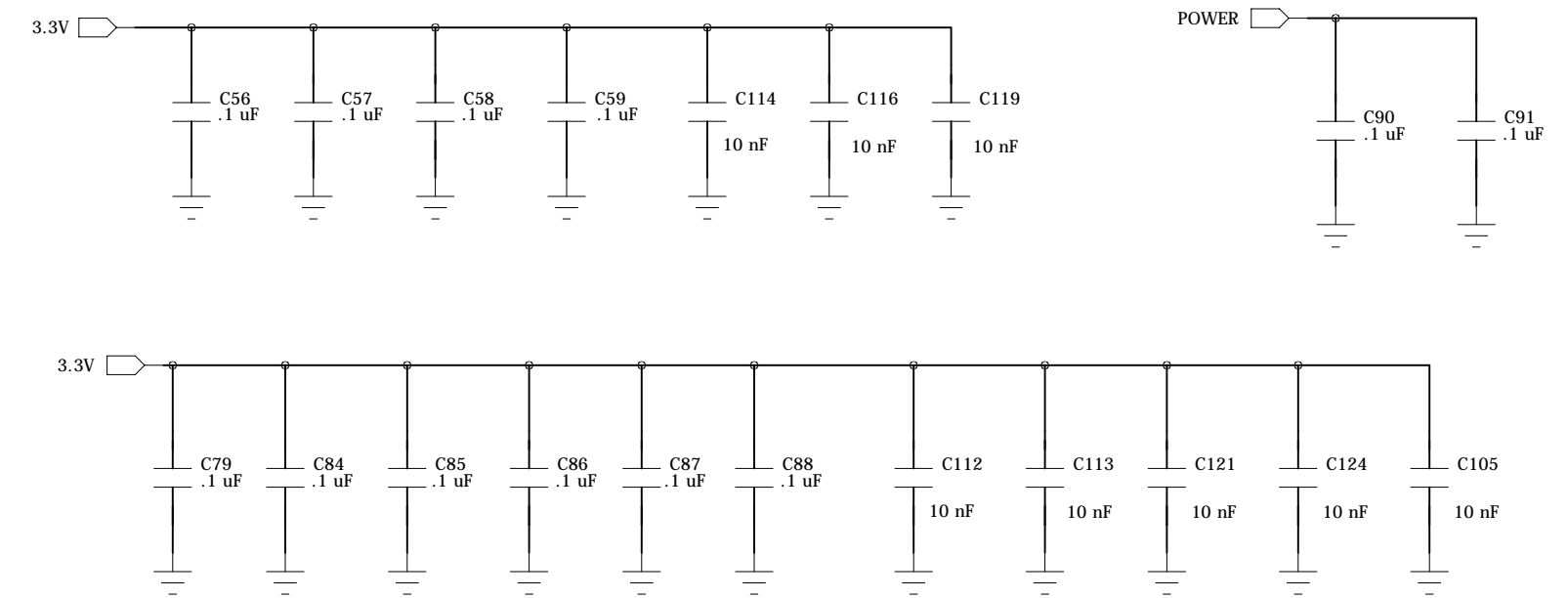
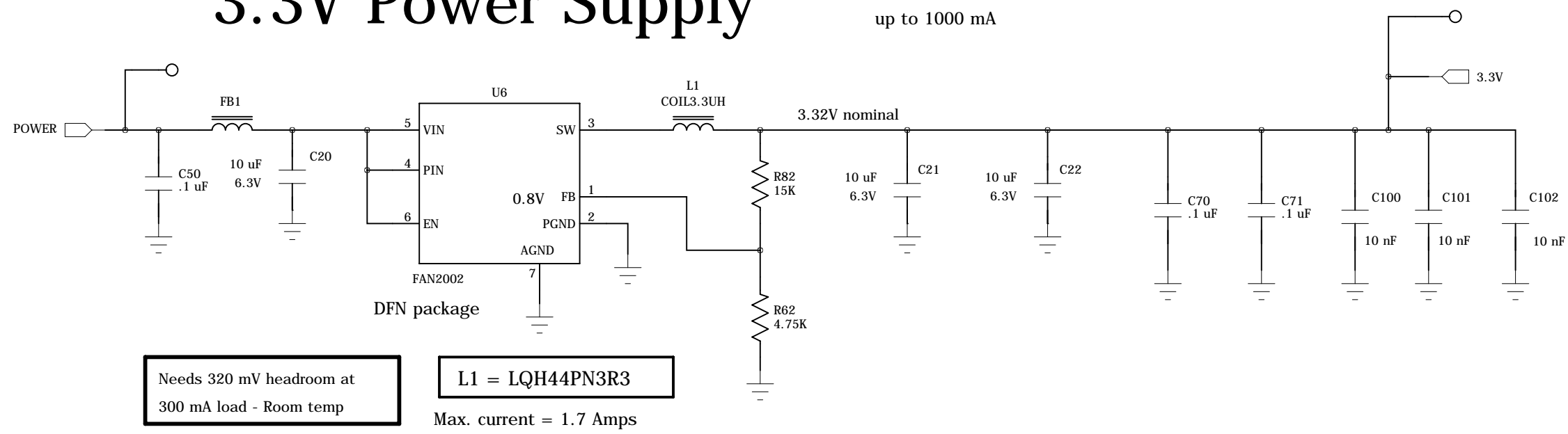
# 64 Mbyte DDR1 SDRAM



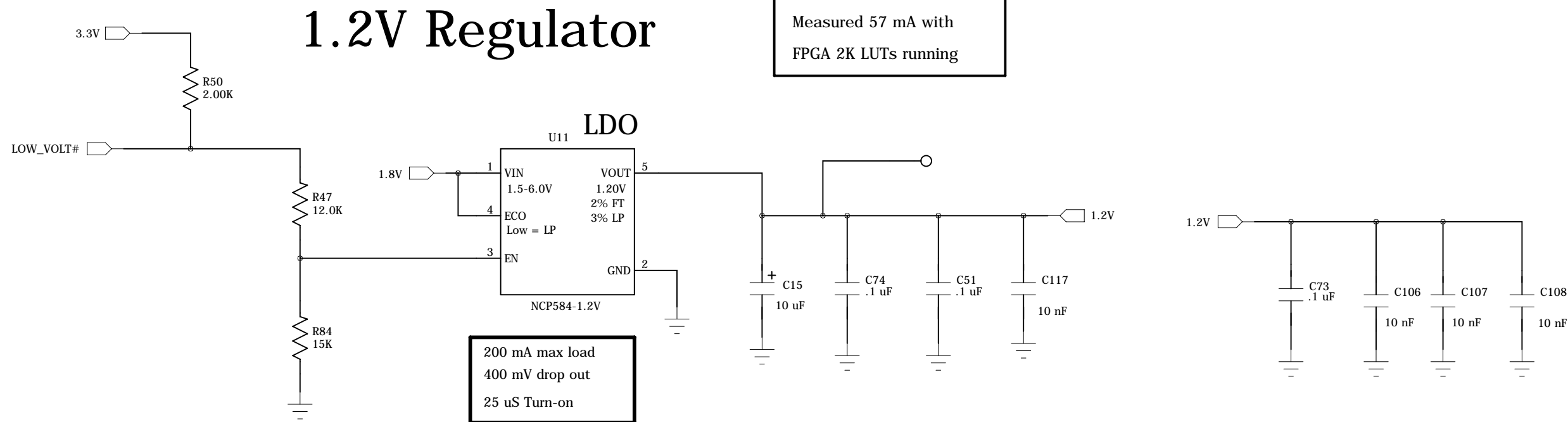
## DDR RAM Notes

- The DDR clock differential pair is the most critical trace on the entire board
- The data lines in each byte lane can be swapped on the RAM chip for optimal layout  
Example: D0 and D5 can be swapped, but not D7 and D8
- The trace length of each data line (in a single byte lane) and the respective QS and DM signals must be matched to within 2.5 mm
- Address and Command signals can be grouped together, but must be isolated from data and M\_DSQ and M\_DM signals (by at least .5 mm)  
Or run them on different layer

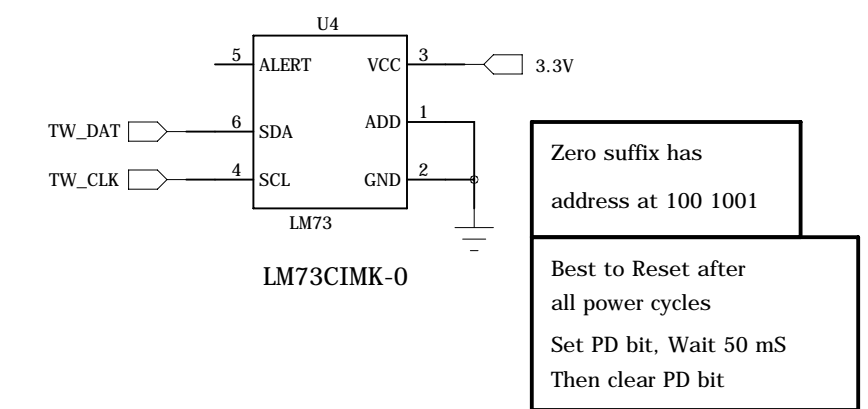
# 3.3V Power Supply



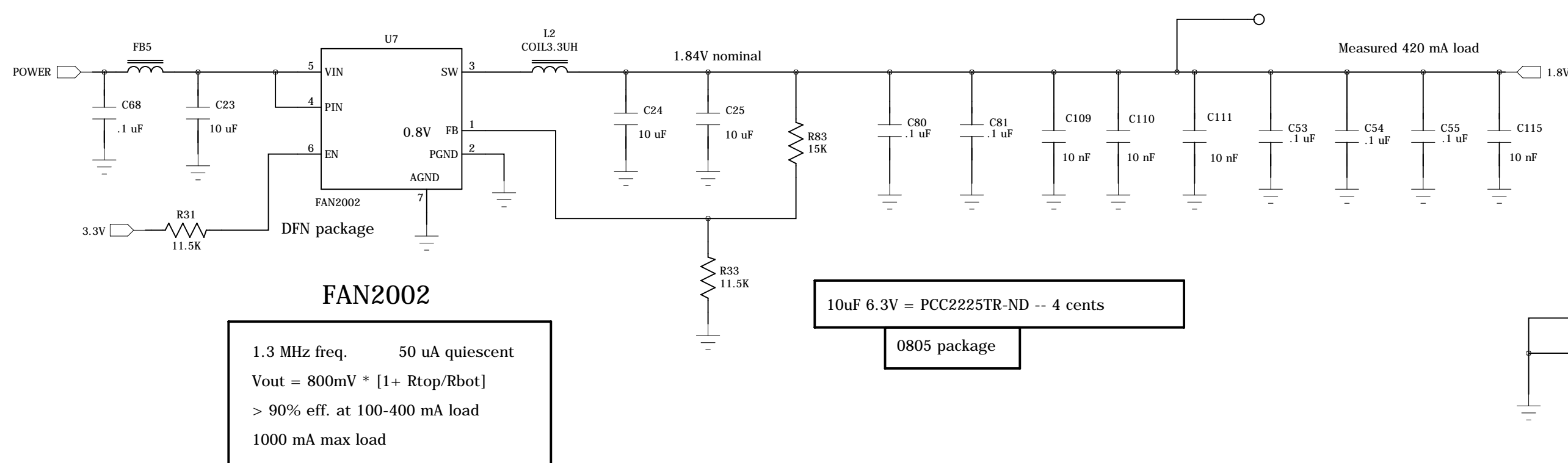
# 1.2V Regulator



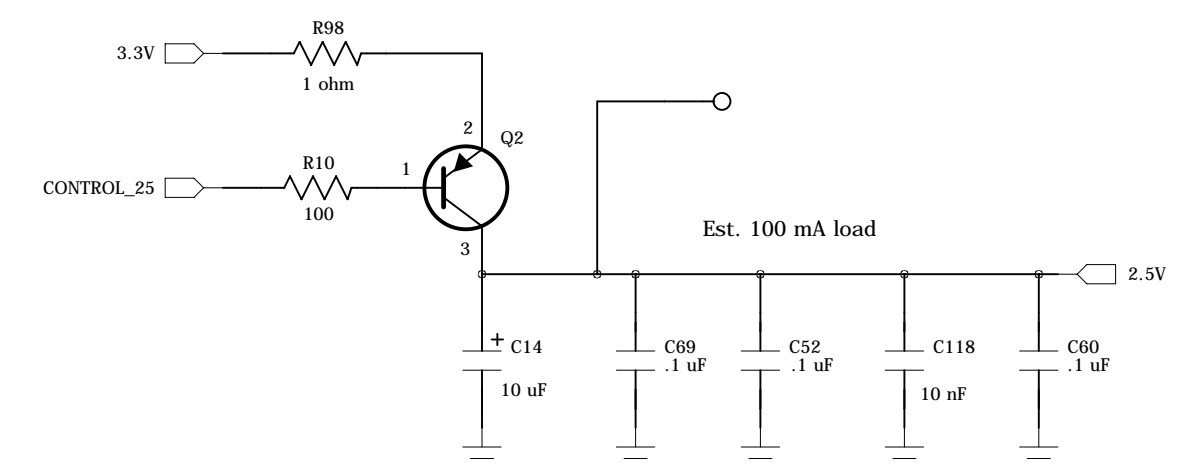
# Temp Sensor



# 1.8V Regulator



# 2.5V Regulator



# Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module  
Apply 3.8V to 5.5V to these pins

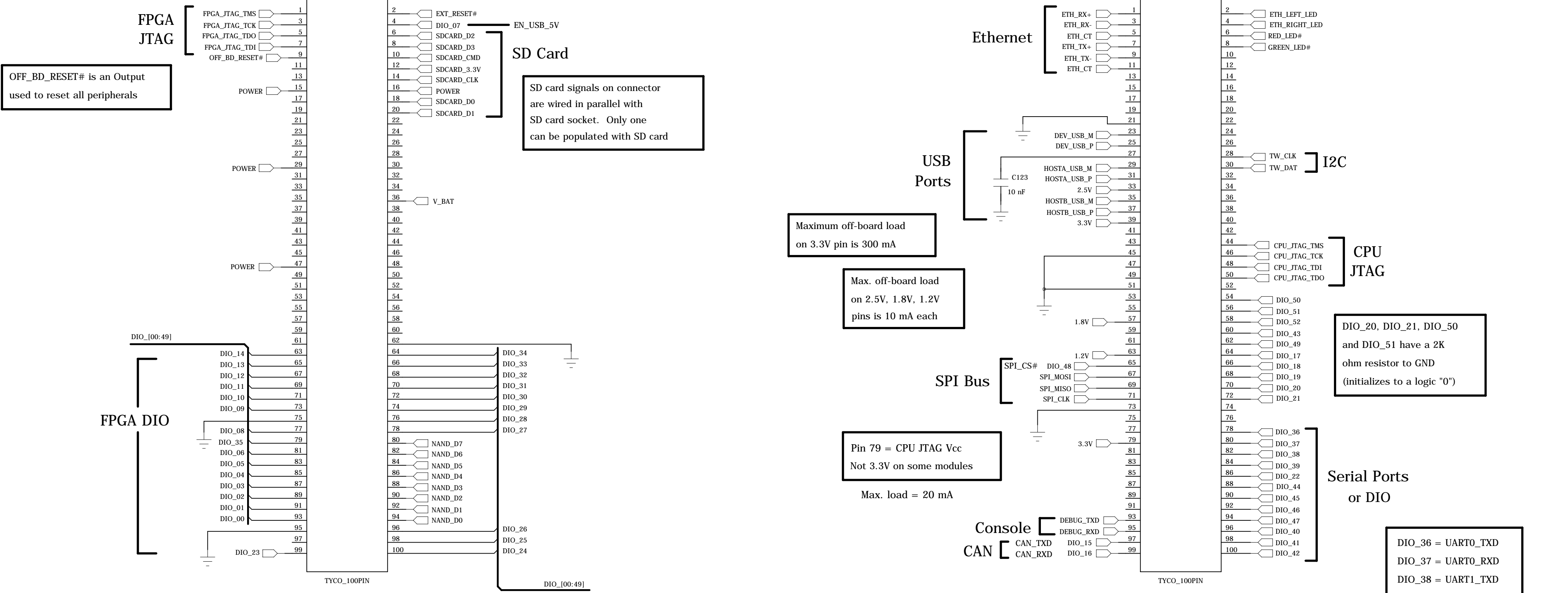
Current drain is approximately 400 mA  
(less than 2 Watts)

EXT\_RESET# is an Input  
used to reboot the CPU

Do not drive active high  
(use open drain)

Left

Right



OFF\_BD\_RESET# is an Output  
used to reset all peripherals

SD card signals on connector  
are wired in parallel with  
SD card socket. Only one  
can be populated with SD card

Maximum off-board load  
on 3.3V pin is 300 mA

Max. off-board load  
on 2.5V, 1.8V, 1.2V  
pins is 10 mA each

Pin 79 = CPU JTAG Vcc  
Not 3.3V on some modules

Max. load = 20 mA

DIO\_20, DIO\_21, DIO\_50  
and DIO\_51 have a 2K  
ohm resistor to GND  
(initializes to a logic "0")

DIO\_36 = UART0\_TXD  
DIO\_37 = UART0\_RXD  
DIO\_38 = UART1\_TXD  
DIO\_39 = UART1\_RXD  
  
DIO\_22 = UART2\_TXD  
DIO\_44 = UART2\_RXD  
DIO\_45 = UART3\_TXD  
DIO\_46 = UART3\_RXD  
  
DIO\_47 = UART4\_TXD  
DIO\_40 = UART4\_RXD  
DIO\_41 = UART5\_TXD  
DIO\_42 = UART5\_RXD

CAN port and all UARTs  
can all be changed  
to simple DIO lines

Mode 1	Mode 2	Boots from
1	1	NAND Flash
1	0	SD Card
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0	0	Off-board Flash

DIO\_26 = MODE1  
DIO\_25 = MODE2

On some other modules, there is a  
16-bit bus for static memory  
type devices. But the TS-4500  
does not support this functionality  
  
The TS-4500 uses these  
"Bus signals" as DIO only.

MODE1 and MODE2 states  
and Board ID bit states  
are latched prior to  
OFF\_BD\_RESET# deasserted

MODE1 and MODE2  
have PU resistors

Use 1K ohm resistor  
to GND to set low

SPI Flash is Boot source  
when MODE1 is low.