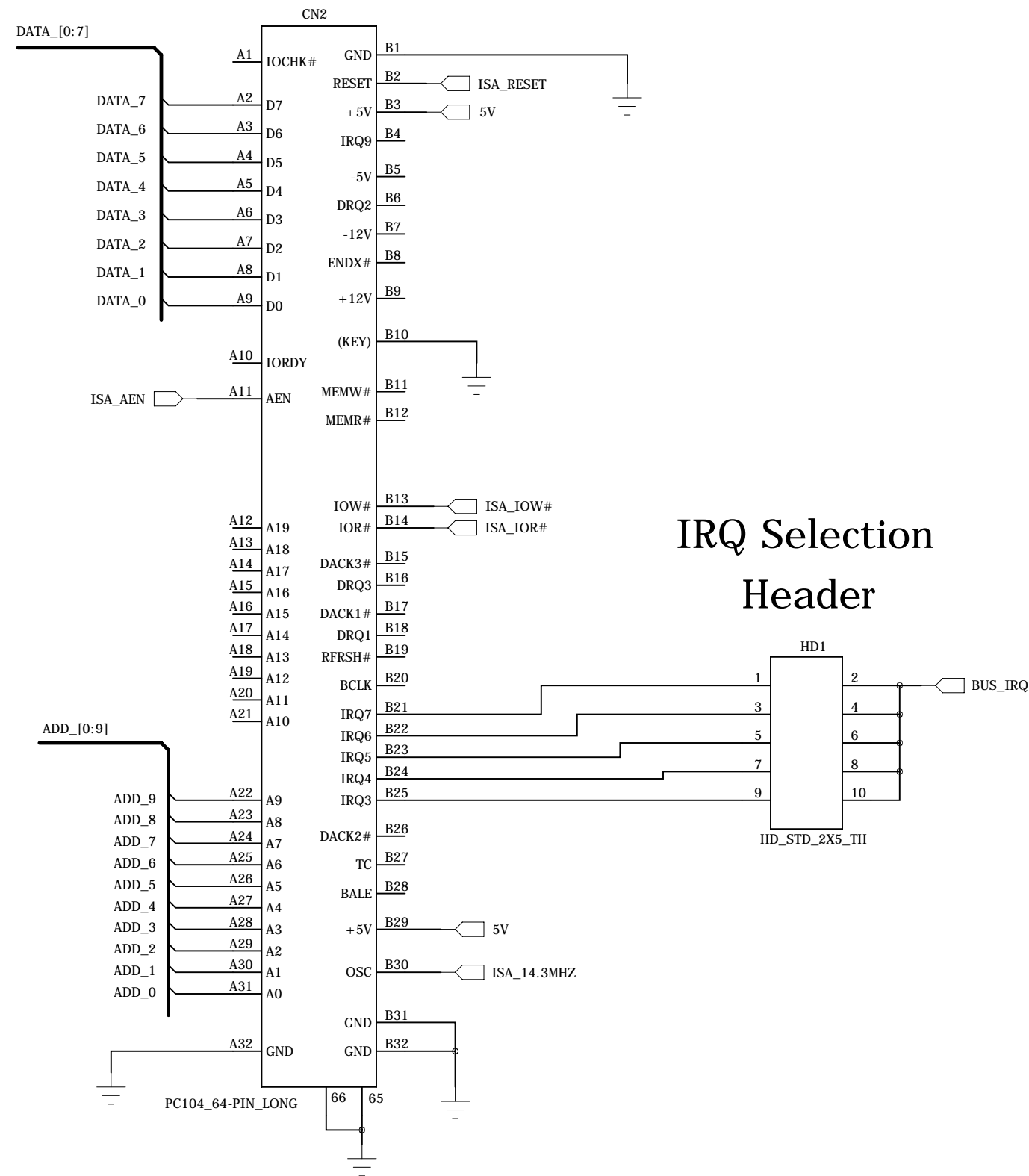
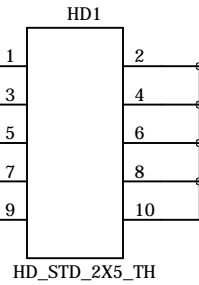


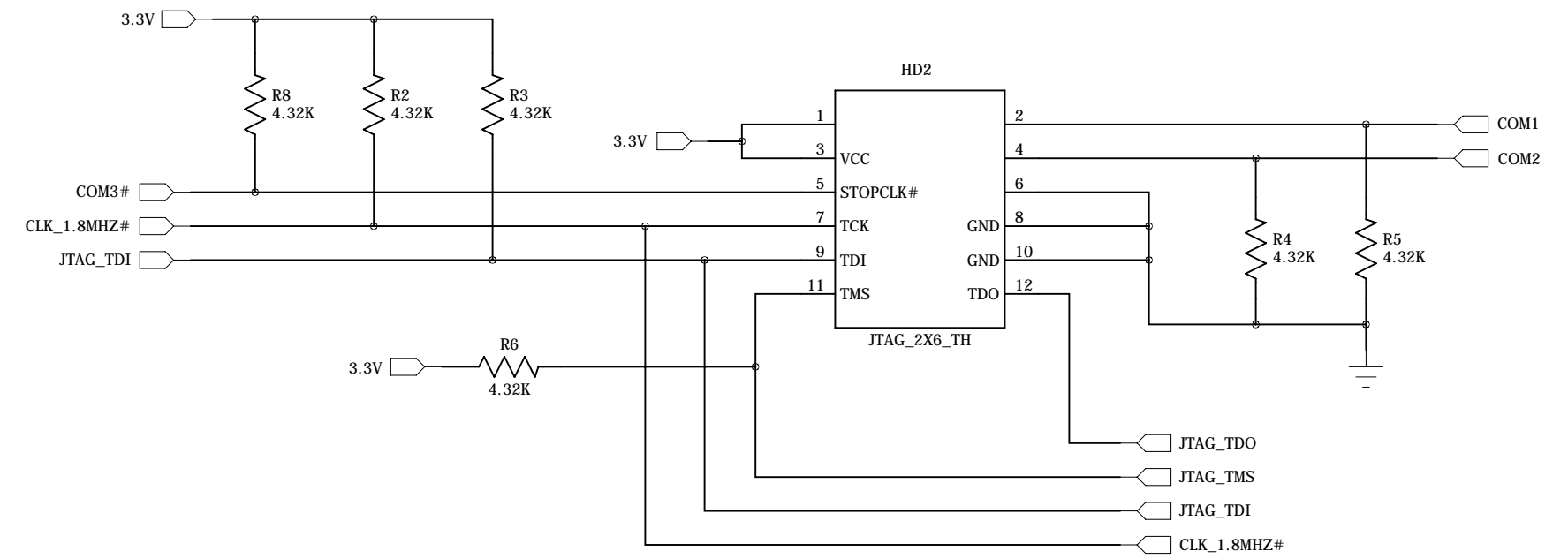
# PC/104 Bus



## IRQ Selection Header

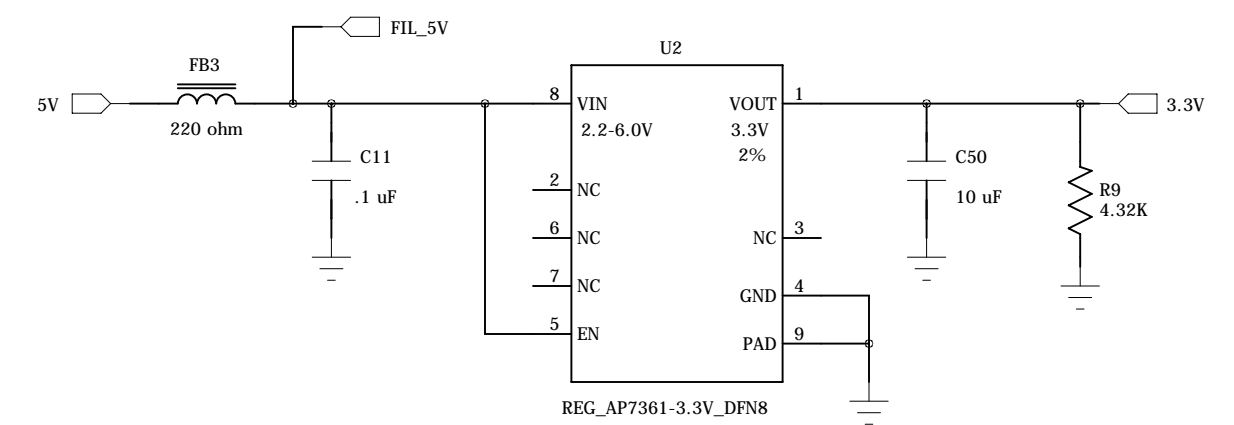


## JTAG

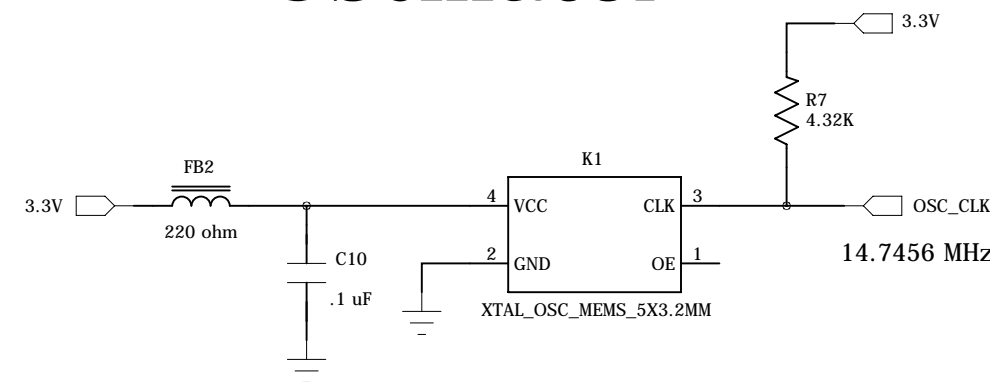


COM4 selected with  
Jumpers COM1 and COM3

## 3.3V Reg.



## Oscillator



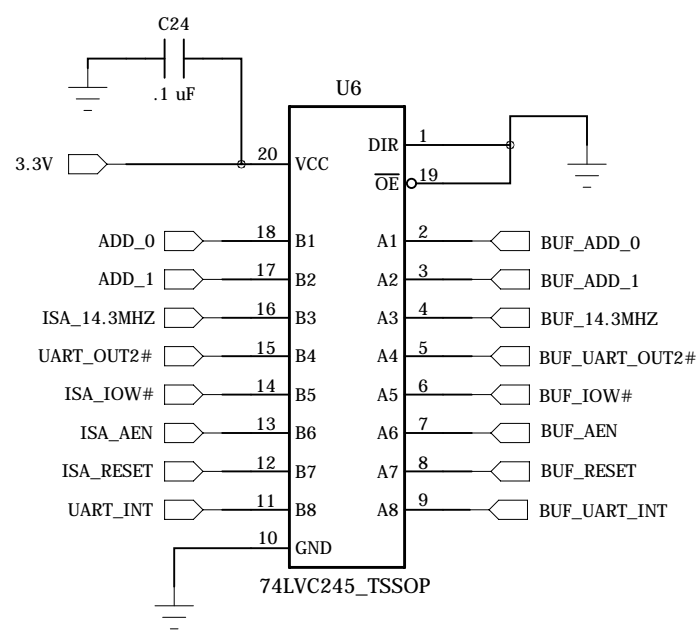
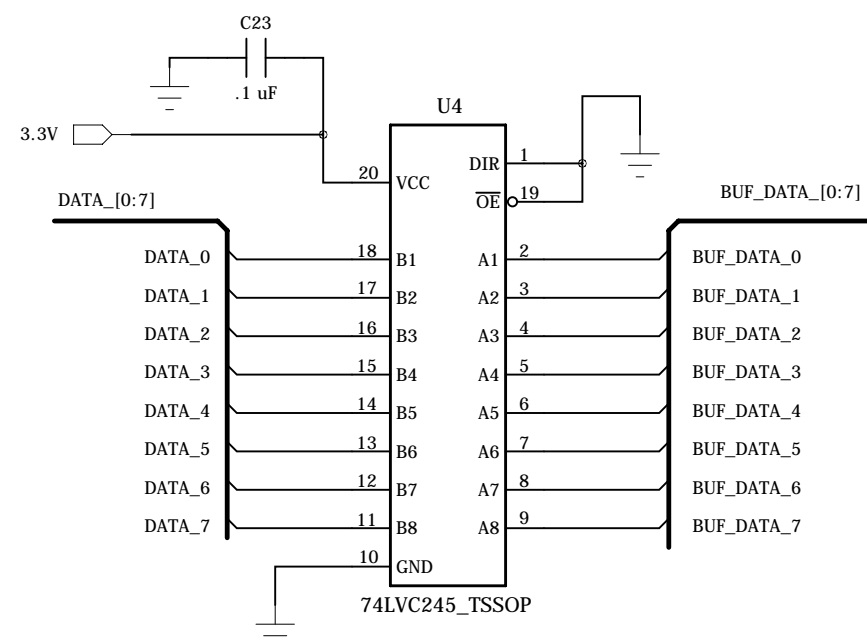
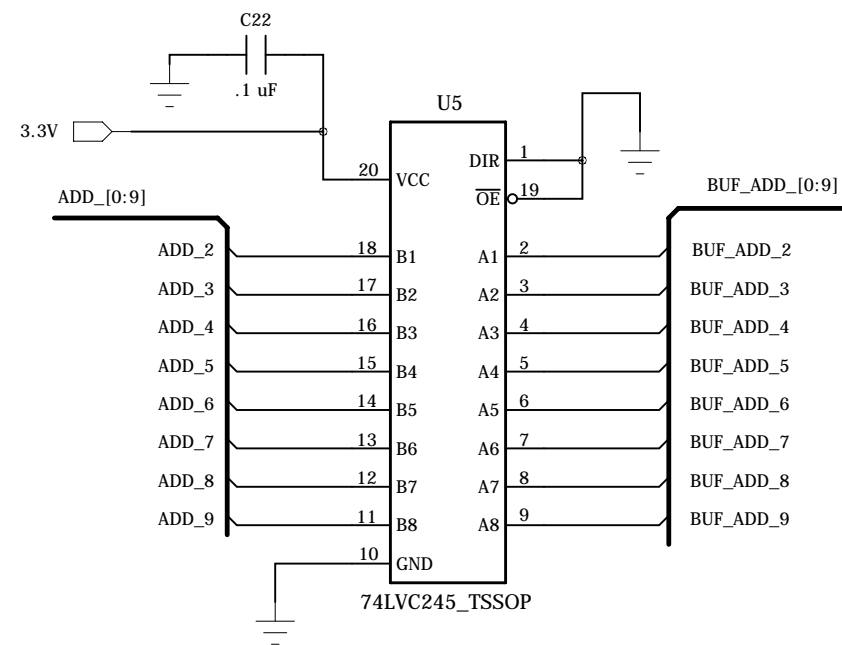
OSC = ASFLMB-14.7456MHZ



Technologic Systems	Date Nov. 19, 2012
Title: TS-Multi_104 PC/104 Bus	
Rev: A	Designer
Sheet 1 of 3	

# Level shifters

5V → 3.3V



# UART Base Address

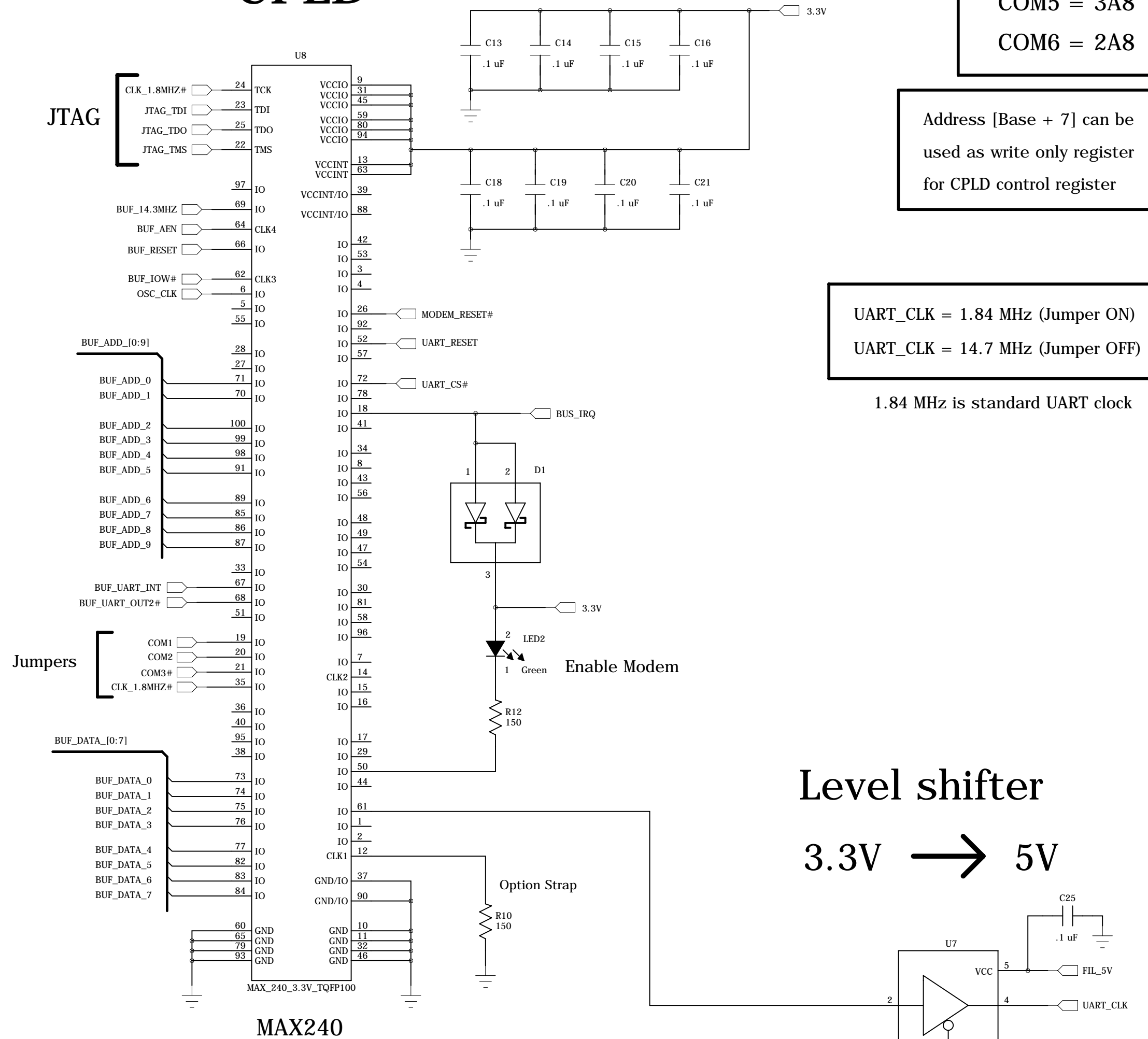
- COM1 = 3F8
- COM2 = 2F8
- COM3 = 3E8
- COM4 = 2E8
- COM5 = 3A8
- COM6 = 2A8

Address [Base + 7] can be used as write only register for CPLD control register

UART\_CLK = 1.84 MHz (Jumper ON)  
 UART\_CLK = 14.7 MHz (Jumper OFF)

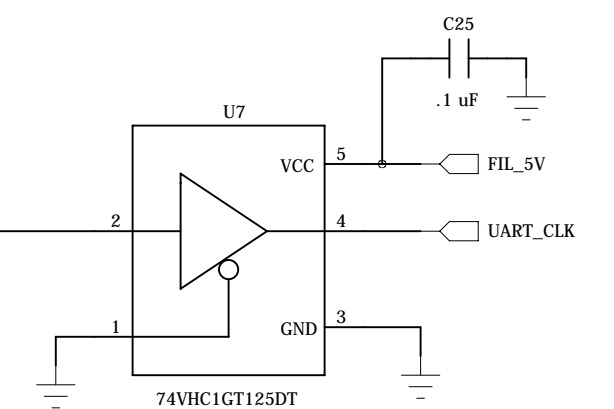
1.84 MHz is standard UART clock

# CPLD



# Level shifter

3.3V → 5V

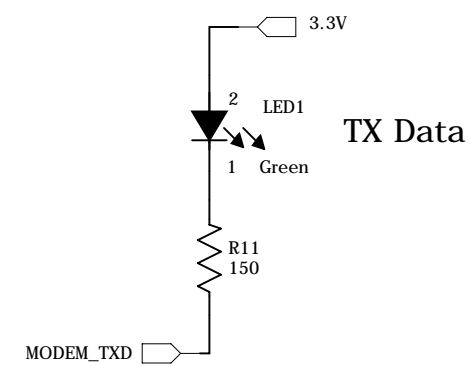
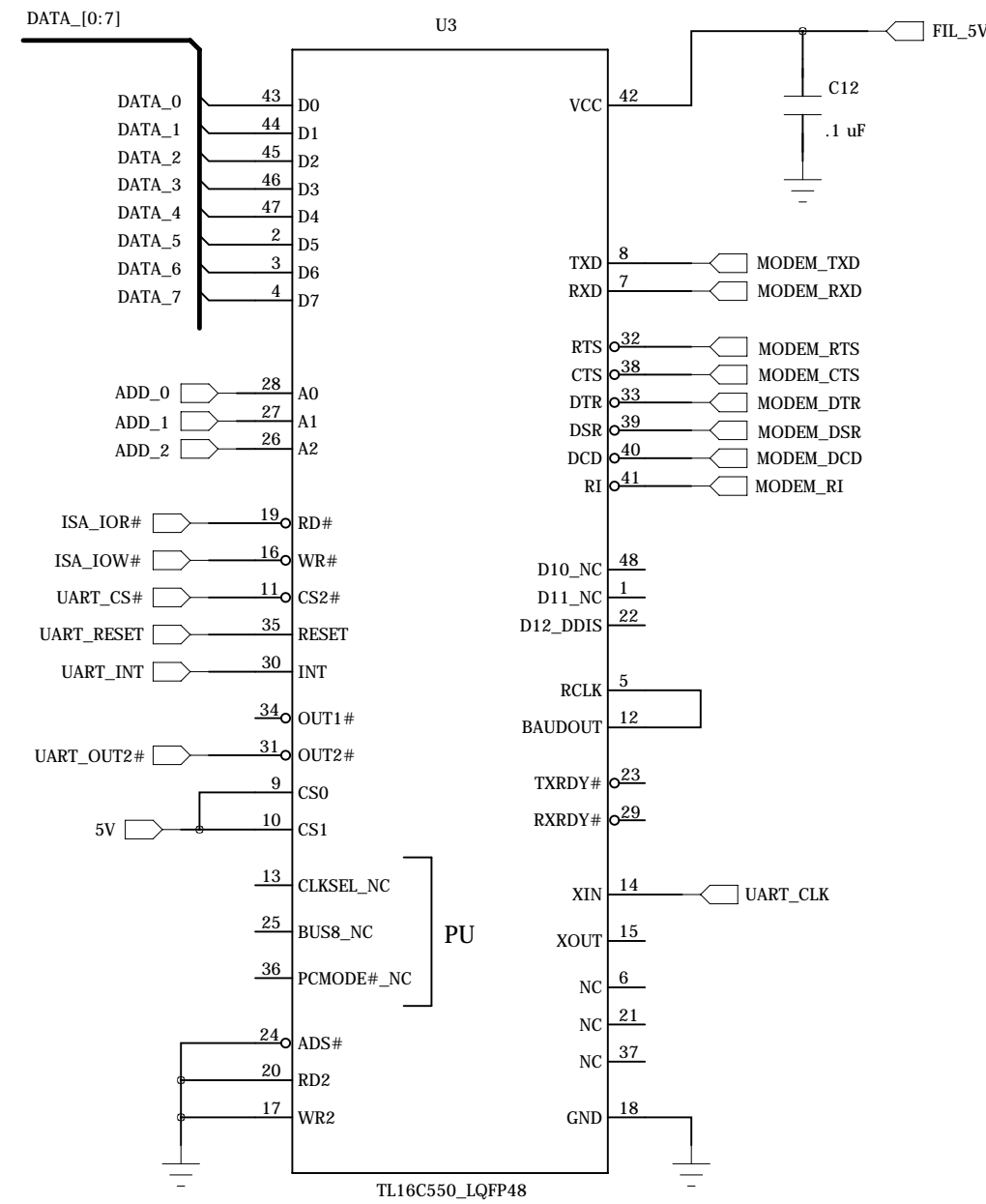


If using PC/104 14.3 MHz

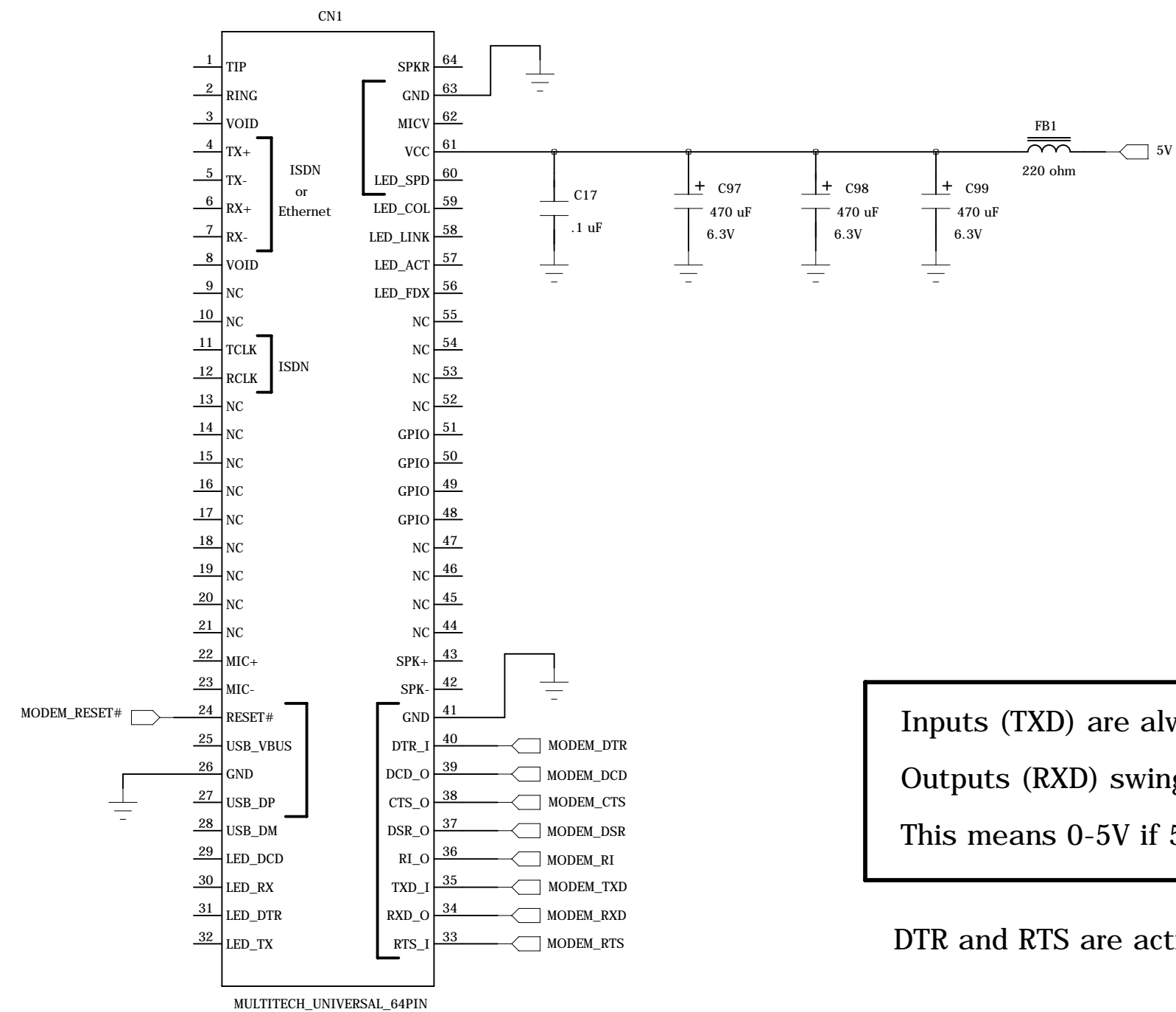
$$14.318 \text{ MHz} \times 4/31 = 1.8475 \text{ MHz}$$

# UART and Multitech Modem

## 16C550 or 16C850 UART



## Multitech Modem



Inputs (TXD) are always TTL compatible  
Outputs (RXD) swing CMOS levels  
This means 0-5V if 5V powered

DTR and RTS are active low true Inputs

TL16C550CIPT max UART\_CLK = 16 MHz  
UART\_CLK min logic high = 3.6V

\$3

XR16C850IM is pin-out same  
and has 128 byte FIFOs  
and UART\_CLK up to 33 MHz  
UART\_CLK min high = 3.0V

\$10

NXP has SC16C650BIB48 in same  
package with 32 byte FIFOs

\$3

NXP has exact same pin-out -- Exar is pin compatible